REMARKS

Claims 1-24 are pending in the present application. By virtue of this response, claims 1 and 17 have been amended, and no claims have been added or deleted. Accordingly, claims 1-24 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented.

Response: Claim Objections

Examiner requested applicants to clarify if a portion of amended claims were inadvertently omitted.

In response, Applicants would like to clarify that this section should be titled "Additional Claim Amendments". This set of claim amendments was made voluntarily by the Applicants to improve the readability of the claims. No new matters were added. In addition, the word "also" should be removed.

Claim Rejections - 35 U.S.C. §101

Claims 1-8 and 17-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

In response, Applicants have amended claims 1 and 17 to include the limitation "storing simulation results of the group of leaf circuits in a memory device." With this amendment, Applicants submit that the rejection of claims 1-8 and 17-24 under 35 U.S.C. 101 should be withdrawn.

The support for this amendment is found in Figure 7 and its corresponding descriptions.

Double Patenting

Claims 1-24 are rejected on the ground of nonstatutory double patenting over claims 1-18 of U.S. Patent No. 7,024,652 (hereinafter the '652 patent) since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

In response, Applicants has previously pointed out in their January 25, 2007 response that the pending claims are distinguished from the '652 patent in at least two aspects: 1) representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior; and 2) creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit; wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits.

Applicants respectfully request the Examiner to reconsider the differences of the claim terms "isomorphic behavior" in the pending application versus the "strength of coupling" in the '652 patent. As explained previously, the isomorphic behavior concerns about the input/output signals, external loads, internal topologies, and internal states of the two leaf circuits. The strength of coupling of two leaf circuits concerns about the connection between two leaf circuits, which may vary from strong (when the connection is in on) to week (when the connection is off). In addition, Applicants have previously pointed out that the dynamic data structure of "first port connectivity interface" is not claimed in the '652 patent.

To further clarify this point, Applicants will address the Examiner Response (Page 5, paragraph 14 of the 4/19/2007 Office Action with two examples. In a first example, if a first inverter and a second inverter demonstrate substantially the same isomorphic behavior, the simulation will take advantage of this information by representing these two inverters with a merged inverter, and the computation will be performed on a single matrix that represent the merged inverter. Thus, the number of computations is reduced. In a second example, if an inverter and an AND gate are weakly coupled (for example a pass-gate transistor between the inverter and the AND gate is off), each of the inverter or the AND gate may be represented by its corresponding matrix for computation. But if the inverter and the AND gate are strongly coupled (for example a pass-gate transistor between the inverter and the AND gate is on), both the inverter and the AND gate may be represented by a matrix that combines the linear equations representing the inverter and the AND gate for a more tightly integrated computation.

Applicants respectfully request the double patenting rejection be withdrawn.

Claim Rejections-35 U.S.C. § 102(e)

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Tcherniaev (US 6,577,992, hereinafter the Tcherniaev reference).

In response, Applicants respectfully request the Examiner to reconsider the reasons previously presented in the January 25, 2007 response. Specifically, Applicants would like to draw the Examiner's attention to the fact that the Tcherniaev reference describes a method of storing dynamic voltage states within each instance of a subcircuit, and such dynamic voltage states information are accessed via pointers of the instance circuits (see Figure 2D of the Tcherniaev reference). All the circuit instances are connected hierarchically in a static circuit storage (see column 3, lines 56-67, and Figure 2 of the Tcherniaev reference). This approach is described in the background section of the pending application (see Figure 6 and its corresponding description). The '992 patent does not describe a dynamically created data structure (port connectivity interface) for communicating changes in signal conditions among the group of leaf circuits selected for simulation. The structure and use of the port connectivity interface is described in Figure 12B and Figure 8B and their corresponding descriptions of the pending application. For the convenience of the Examiner, Applicants hereby list the previously presented reasons below.

Applicants submit that one of the key differences between the current invention and the Tcherniaev reference lies in how dynamic information among the circuit components under simulation is communicated and what data structure are used for communicating such dynamic information during a transient simulation. It is known in the art that during a simulation, the simulator needs to keep track of port connectivity information of the circuit components. It is also known that during a simulation, the circuit components will go through different dynamic states. So the issue is not whether the port connectivity information or dynamic states exist or not, but how are they stored or used by the simulator.

In the Tcherniaev reference, it chose to store such information in the static database while the current invention uses a newly created dynamic data structure called the port connectivity

interface for storing and communicating such dynamic information during simulation. However, there is major design tradeoffs involved in each implementation approach. The pending application describes the Tcherniaev approach in Figure 6 and its corresponding paragraphs [0018] – [0020] in the background section of the specification. In particular, the Tcherniaev approach employs pointers to pass such dynamic information through the subcircuit instances (See Figure 2C of Tcherniaev.) Therefore, to pass information from one subcircuit to the next subcircuit in a different hierarchical branch, such as from subcircuit 620 to subcircuit 622 as shown in Figure 6 of the pending application, the simulator of the Tcherniaev reference would have to made multiple program calls (via the pointers). As indicated in the background section of the pending application, the problem with the method taught by Tcherniaev reference is that the dynamic information needs to traverse many levels of the hierarchical data structure before reaching its destination. At each hierarchical level, information needs to be synchronized before it may be transmitted to the next level, which the Tcherniaev reference are totally silent about these design issues. Therefore, the method of passing information through the hierarchies, as taught by Tcherniaev, and synchronizing at each intermediate level would result in lower simulation performance.

The Office Action cites column 4 lines 44-47, Fig. 2B-2D, and Fig. 3 allegedly teach these claim elements, Applicants respectfully disagree. Applicants respectfully submit that merely mentioning the terms "port connectivity" does not indicate a particular approach used by the simulator. On the contrary, the Tcherniaev reference teaches a different approach for storing and handling dynamic information created during the simulation. For example, the Tcherniaev teaches that "[T]he static storage may therefore store the matrix structure. As described above, the static subcircuit storage 212 may further include a subcircuit definition 217 that defines the subcircuit topology. In addition, the static subcircuit storage 212 may provide element definitions 219 associated with the subcircuit definition 217." (See Tcherniaev, column 9, lines 50-55, emphasis added.) The Tcherniaev also teaches that "[I]t is important to note that the circuit simulation is advantageously accomplished by traversing a hierarchical data structure such as that illustrated in FIG. 2A without flattening the hierarchical data structure." (See Tcherniaev, column 10, lines 7-10, emphasis added.) The Tcherniaev further states that "[I]n addition to sharing an equivalent circuit structure and therefore static subcircuit storage, two subcircuit instances may have an equivalent

dynamic voltage state obtained during transient simulation. As shown in FIG.2C, multiple instances 224, 226, 228 of the same subcircuit definition may share the same static subcircuit storage 212 as described above." The Tcherniaev reference further teaches that "one or more pointers ... may be used to permit both the first instance 224 and the third instance 228 to share this dynamic voltage state." (See Tcherniaev, column 10, lines 17-33, emphasis added.) Applicants also note that column 14 lines 39-54 and column 16 line 35 to column 17 line 47 of the Tcherniaev reference teaches updating rate of change in node voltage, again by using pointers to traverse the hierarchical data structure. It is clear that the Tcherniaev reference teaches storing dynamic simulation information in the static subcircuit storage and using pointers to traverse the hierarchical data structure for passing dynamic information among subcircuits under simulation. The Tcherniaev reference is totally silent about the design issues, such as multiple program calls and synchronization between hierarchies, associated with its approach. No dynamic data structure, such as the port connectivity interface, is created by the Tcherniaev reference in response to the isomorphic behavior of the group of leaf circuits under simulation. The present invention addresses these design issues by using the port connectivity interface to facilitate communication of dynamic information among circuit components under simulation.

For at least the reasons presented above, Applicants respectfully submit that the Tcherniaev reference does not disclose each and every element of the independent claims 1, 9, and 17. Applicants also assert that claims 2-8, 10-16, and 18-23, which variously depend from their independent claims, are allowable for at least the reason that they depend from allowable independent claims.

With respect to claims 5, 13, and 21, Applicants respectfully submit that the Tcherniaev reference does not disclose at least the element "splitting the merged leaf circuits into two or more individual leaf circuits in response to the two or more leaf circuits represented by the merged leaf circuit demonstrating substantially different isomorphic behaviors; creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits; wherein the second port connectivity interface communicates changes in signal conditions among the group of leaf circuits."

Based on the arguments presented above, Applicants have established that the Tcherniaev reference does not disclose the solution of creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit to address the situation when leaf circuits in a transient simulation are merged. For the same reasons presented above, the Tcherniaev reference does not disclose the solution of creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits to address the situation when a merged leaf circuit in a transient simulation are split into two or more individual leaf circuits.

Applicants respectfully request the rejection under 35 U.S.C. 102(e) be withdrawn.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no.188122001700. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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